Graphics Programming Conference 2025, Breda

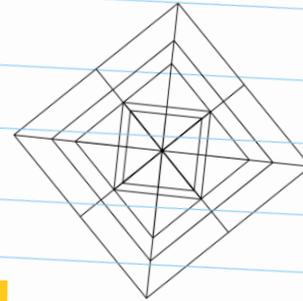The optimization process

Profiling in PIX

Intel + PIX

Steven Tovey
Intel

Define

Understand

Diagnose

0

3

1

4

5

2

Validate

Implement

Analyse

In-depth shader profiling

XVE stall sampling,
with per-instruction visualisation
of stall reasons.

First class metrics experience

Stabilize, consolidate, and organize
HW & derived metrics for ease of
profiling.

Crash debugging

Make it easier to diagnose root cause
of GPU crashes and hangs.

This swim lane guides us into areas which need our attention...

Shows utilization of different parts of our Xe GPU.

This swim lane guides us into areas which need our attention...

Choosing a focus area...

- Is it representative of my application?

- Is it taking a chunk of frame?

vs utilization of ferent parts of ur Xe GPU.

Might as well start here, but first...

First level of grouping is called a "Render Slice".

Inside a Render Slice we have a number of XᵉCores...

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... and each XeCore has a number of Xe Vector Engines.

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Each XVE can have up to 8 threads.

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Each XVE can have up to 8 threads.

General formula for GPU thread count:

Render slice x XeCore per slice x XVE per XeCore x Threads per XVE

Each XVE can have up to 8 threads.

Intel® B580 (aka "Battlemage"):

5 Render slice x 4 XeCore per slice x

8 XVE per XeCore x 8 Threads per XVE

1280

Almost no GPU threads...

"Thread Dispatcher Starved"

Fetcher is working very hard...

Clipper is also strained...

Select stats relating to quantities in the pipeline, then click the arrow and select "Save As"

Let's shift gears and have a peek at this...

Filling the GPU up with threads, that's good right?

XVE Stalled
+
XVE Active
=
XVE Busy

...but are more threads <u>always</u> better?

XVE Thread Occupancy

XVE busy

intel

XVE Stalled
+
XVE Active
=
XVE Busy

$\rho\ XVE_{active}\ ,\ XVE_{occupancy}$

~0.132

$\rho\ XVE_{busy}\ ,\ XVE_{occupancy}$

~0.685

Pearson of 0 is not correlated, 1 is highly correlated.

...but are more threads <u>always</u> better?

◉_◉

XVE Thread Occupancy

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$$\rho_{XVE_{active},\ XVE_{occupancy}}$$

~0.132

$$\rho_{XVE_{busy},\ XVE_{occupancy}}$$

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Pearson of 0 is not correlated, 1 is highly correlated.

Remember: Threads are just another tool to achieve your goal. Not the goal itself.

...but are more threads <u>always</u> better?

XVE Thread Occupancy

XVE busy

ಠ_ಠ

XVE Stalled

XVE Active

XVE Idle

XVE Active is a better proxy for our true goal.

Input ⟹ X-form ⟹ Output

The faster this goes, the more interactivity we achieve.

Use more resources

Use resources better

X-form

Simplify

Reformulate

Resources are things like "compute horsepower" and "memory".

Using more available resources can speed up transformations.

Input ⟹ X-form ⟹ Output

The faster this goes, the more interactivity we achieve.

XVE Stalled

XVE Active

XVE Idle

… So, what's with the purple and white?

We can see the reasons that the XVE was stalled

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XVE stall reasons

Control	Data
	Scoreboard ID
Instruction fetch	ALU write
Barrier	GRF Read stall
Control	Pixel shader dep.
Send write	Other

Instruction fetch stall

If there are no instruction cache lines available for a thread, then we can't run any code for that thread.

Instruction fetch stall

Message dependency

Thread controller → Message execution unit

FIFO inside here can get filled up.

Messages take time to be handled by their target shared function.

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Jump dependency

Jump execution unit → jump address → Instruction queue

I$ ↑

When we don't yet know the new instruction pointer, we can't execute code.

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XVE stall reasons

Control	Data
	Scoreboard ID
~~Instruction fetch~~	ALU write
Barrier	GRF Read stall
~~Control~~	Pixel shader dep.
~~Send write~~	Other

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Address	Opcode	Destination
0x00000000	add	r0
0x00000010	add	r2
0x00000020	add	r6
0x00000030	add	r8
0x00000040	send	r10
0x00000050	sync.nop	
0x00000060	add	r6
0x00000070	add	r12

Source 0	Source 1
r20	r21
r22	r23
r2	r21
r0	r21
r6	
r0	r21
r10	r8

Register Distance	Scoreboard
-	-
-	-
1	-
-	-
2	$0
-	-
-	$0.src
2	$0.dst

Address	Opcode	Destination	Source 0	Source 1	Register Distance	Scoreboard
0x00000000	add	r0	r20	r21	-	-
0x00000010	add	r2			-	-
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0x00000030	add	r8			-	-
0x00000040	send	r10			2	$0
0x00000050	sync.nop				-	-
0x00000060	add	r6			-	$0.src
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Instruction syntax

Scoreboard dependency

(simd) op d, s0, s1, s2 {rd, $sb}

Register distance

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Out-of-order   In order

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In-order
RAW

Out-of-order   In order

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In-order RAW
Out-of-order RAW
Out-of-order WAR

Out-of-order   In order

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Thread Dispatcher

Xᵉ Vector Engine (XVE)

core

Group Shared Memory is allocated from the L1 by the thread dispatcher.

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Instruction data

Threads & payloads

Dataport

Level 1 Cache

Level 2 Cache

numthreads(8,8,1)

Thread group

HW Thread

We need a sync primitive (a barrier) to ensure access to the shared memory is synchronized.

Sampler

Sampler Cache

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2025

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XVE stall reasons

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~~Send write~~	Pixel shader dep.
	Other

We're not seeing high XVE stall here, but still seeing stall reasons... What gives?

Remember the goal!

Hint:
Eliminating XVE
stalls is not it.

To do list:

- Know the optimization process
- Define goals, and focus on them
- Know my tools
- Understand the substrate
- Aim for 100%, but stop at ~95%
- Optimize regularly

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Minimize data transformation energy.

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Thread occupancy is less useful than XVE utilization, but more useful than a sandwich.

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Feedback always welcome!

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askwinpix@microsoft.com

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- Results that are based on pre-production systems and components as well as results that have been estimated or simulated using an Intel Reference Platform (an internal example new system), internal Intel analysis or architecture simulation or modeling are provided to you for informatio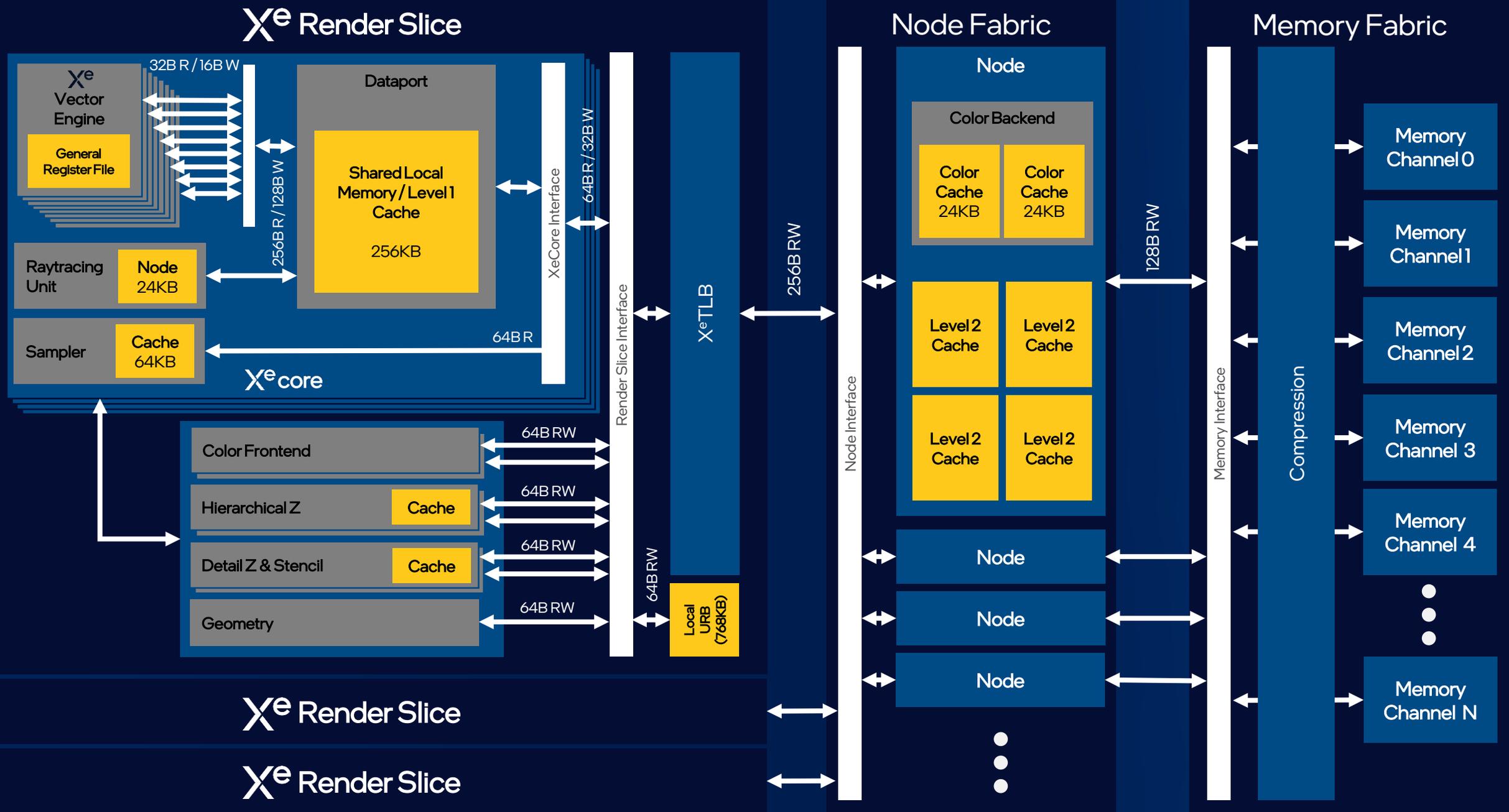nal purposes only. Results may vary based on future changes to any systems, components, specifications or configurations.

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